GENERAL DESCRIPTION

The CT7602 is a single chip audio USB 2.0/1.1 payback and record bridge.

FEATURES

- 1 playback port, and 1 record port
  PLAY: 2-channel I2S, 2-channel DSD, 2-channel SPDIF
  RECORD: 2-channel I2S, 2-channel DSD
  The clock systems are independent
- I2S Interface
  PLAY port supports standard/left justified format, master mode.
  RECORD port supports standard/left justified, master/slave mode.
- Audio transmission
  PCM support up to 768K/32bit through USB, I2S, SPDIF ports.
  DSD (PDM) support 1x/2x/4x/8x bandwidth through DSD(PDM) port.
  DSD (Native) support 1x/2x/4x/8x bandwidth through USB, I2S, DSD(PDM) , SPDIF ports.
  DoP support 1x/2x/4x bandwidth through USB, I2S, SPDIF ports.
- Interface
  Up to 16 GPIOs configurable as input or output.
  Master / Slave I^2C interface.
  3 PWM-LED.
- Format auto detecting
  Auto detecting PCM / DoP format.
  Auto detecting I2S / DSD interface.
- Misc
  UART interface
  Volume control with fading in/out function.
  Playback basic auto De-pop function.
  One 12MHz crystal requirement only.
  Digital MIC input acceptable.
  2 External OSC select for output PLL

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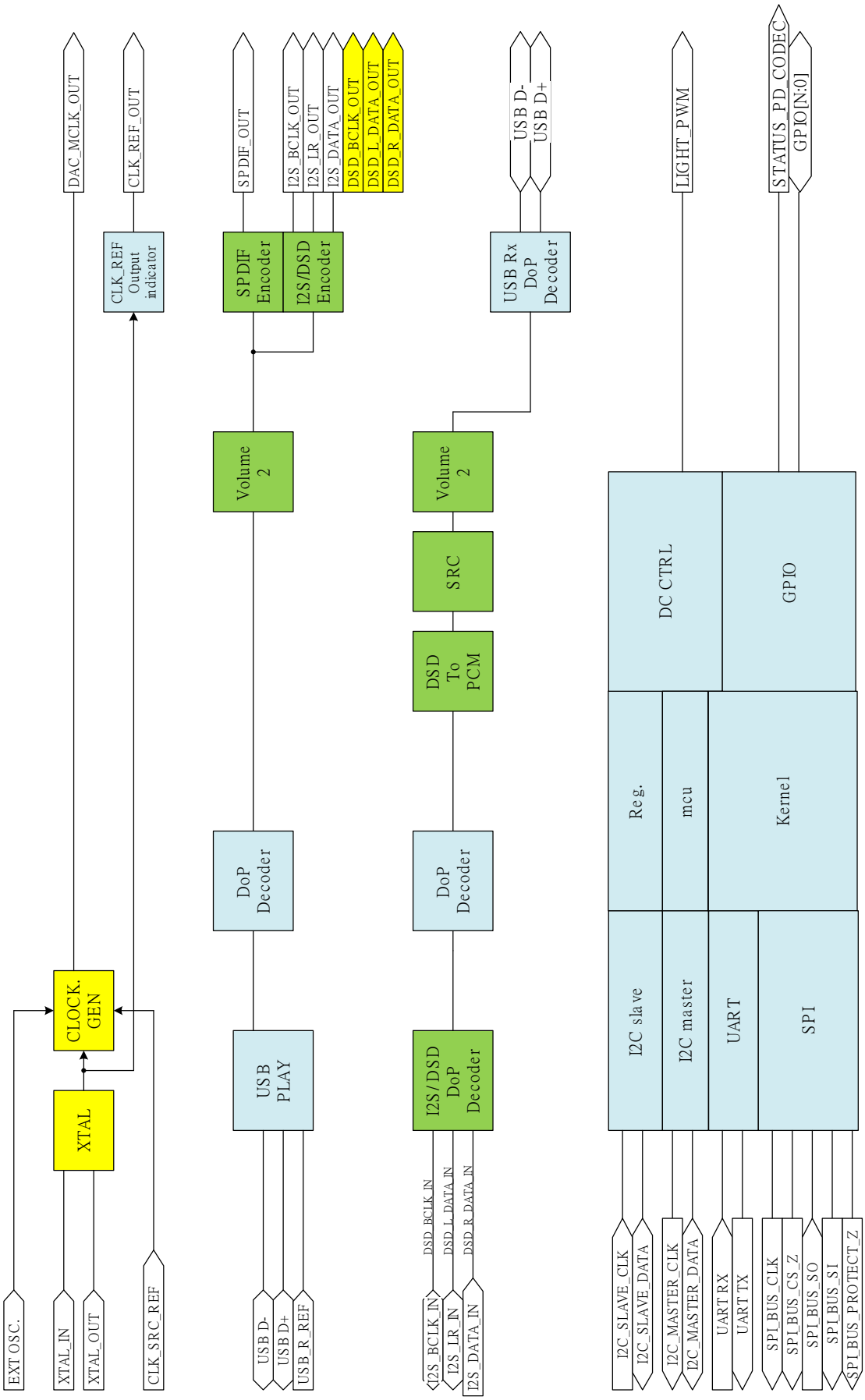
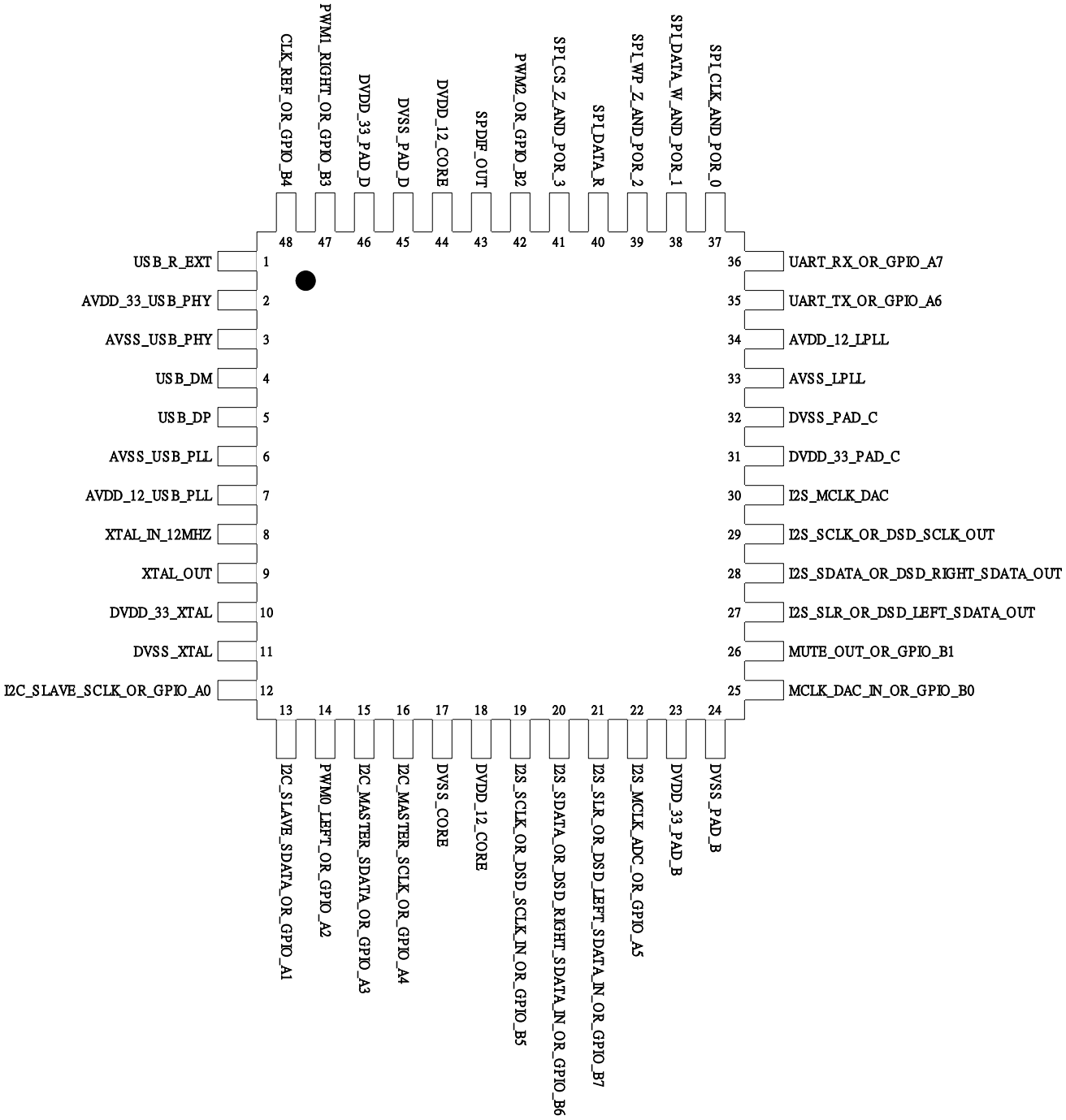
FUNCTION BLOCK



CT7602 FAMILY

Description	CT7602PR	CT7602CR	CT7602SR
USB Port PLAY / RECORD			
USB PCM	768kHz / 32-bit	384kHz / 32-bit	192kHz / 32-bit
USB DoP	4x	2x	1x
USB DSD	8x	4x	2x
I2S Port			
I2S PCM	768kHz / 32-bit	384kHz / 32-bit	192kHz / 32-bit
I2S DoP	4x	2x	1x
Native DSD	8x	4x	2x
SPDIF Port			
SPDIF PCM	768kHz / 32-bit	384kHz / 32-bit	192kHz / 32-bit
SPDIF DoP	4x	2x	1x
SPDIF native DSD	8x	4x	2x
Package			
Package	QFN 48		
GPIO	16		
SPDIF Play channel	2		

Package QFN-48 (Top View) CT7602xR



QFN 48 PIN DESCRIPTION

Pin Name	Pin No.	Type	Description
USB_R_EXT	1	I	***USB external resistor :*** 1.8k ohm (1%) pull low
AVDD_33_USB_PHY	2	P	***3.3V Pad Power Connection:*** Power supply for USB physical layer. Connect to 3.3V.
AVSS_USB_PHY	3	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
USB_DM	4	I/O	***USB D - :*** refer to USB Specification.
USB_DP	5	I/O	***USB D + :*** refer to USB Specification.
AVSS_USB_PLL	6	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
AVDD_12_USB_PLL	7	P	***1.2V Core Power Connection:*** Power supply for USB PLL function. Connect to 1.2V.
XTAL_IN_12MHZ	8	I	***External Crystal input:*** Connect to external crystal pin. Or external clock input. Selection : 12 MHz
XTAL_OUT	9	O	***External Crystal output:*** Connect to external crystal pin
DVDD_33_XTAL	10	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
DVSS_XTAL	11	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
I2C_SLAVE_SCLK_OR_GPIO_A0	12	I/O	***I2C slave serial clock :*** Clock pin for serial interface. Refer to I2C specification. ***General purpose input/output pin bank_A[0] :*** 3.3V TTL input/output pin, define by internal control register.
I2C_SLAVE_SDATA_OR_GPIO_A1	13	I/O	***I2C slave serial data :*** Data pin for serial interface. Refer to I2C specification. ***General purpose input/output pin bank_A[1] :*** 3.3V TTL input/output pin, define by internal control register.
PWM0_LEFT_OR_GPIO_A2	14	I/O	***PWM0 light control output :*** refer to programming guide ***General purpose input/output pin bank_A[2] :*** 3.3V TTL input/output pin, define by internal control register.
I2C_MASTER_SDATA_OR_GPIO_A3	15	I/O	***I2C master serial data :*** Data pin for serial interface. Refer to I2C specification. ***General purpose input/output pin bank_A[3] :*** 3.3V TTL input/output pin, define by internal control register.
I2C_MASTER_SCLK_OR_GPIO_A4	16	I/O	***I2C master serial clock :*** Clock pin for serial interface. Refer to I2C specification. ***General purpose input/output pin bank_A[4] :*** 3.3V TTL input/output pin, define by internal control register.
DVSS_CORE	17	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
DVDD_12_CORE	18	P	***1.2V Core Power Connection:*** Power supply for all digital function. Connect to 1.2V.
I2S_SCLK_OR_DSD_SCLK_IN_OR_GPIO_B5	19	I/O	***I2S serial clock input :*** 3.3V TTL input, refer to I2S Specification. ***DSD serial clock input :*** 3.3V TTL input, refer to DSD Specification. ***General purpose input/output pin bank_B[5] :*** 3.3V TTL input/output pin, define by internal control register.

Pin Name	Pin No.	Type	Description
I2S_SDATA_0_OR_DSD_RIGHT_SDATA_IN_OR_GPIO_B6	20	I/O	***I2S serial data0 input :*** 3.3V TTL input, refer to I2S Specification. ***DSD serial right data (channel 1) input:*** 3.3V TTL input, refer to DSD Specification. ***General purpose input/output pin bank_B[6] :*** 3.3V TTL input/output pin, define by internal control register.
I2S_SLR_OR_DSD_LEFT_SDATA_IN_OR_GPIO_B7	21	I/O	***I2S left/right input :*** 3.3V TTL input, refer to I2S Specification. ***DSD serial left data (channel 0) input:*** 3.3V TTL input, refer to DSD Specification. ***General purpose input/output pin bank_B[7] :*** 3.3V TTL input/output pin, define by internal control register.
I2S_MCLK_ADC_OR_GPIO_A5	22	I/O	***I2S master clock output:*** 3.3V TTL output, refer to ADC Document. ***General purpose input/output pin bank_A[5] :*** 3.3V TTL input/output pin, define by internal control register.
DVDD_33_PAD_B	23	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_B	24	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
MCLK_DAC_IN_OR_GPIO_B0	25	I/O	***I2S master clock input:*** 3.3V TTL input, refer toDAC Document. ***General purpose input/output pin bank_B[0] :*** 3.3V TTL input/output pin, define by internal control register.
MUTE_OUT_OR_GPIO_B1	26	I/O	***Mute sigmal output:*** 3.3V TTL output, refer to DAC Document. ***General purpose input/output pin bank_B[1] :*** 3.3V TTL input/output pin, define by internal control register.
I2S_SLR_OR_DSD_LEFT_SDATA_OUT	27	O	***I2S left/right output :*** 3.3V TTL output, refer to I2S Specification. ***DSD serial left data (channel 0) output:*** 3.3V TTL output, refer to DSD Specification.
I2S_SDATA_OR_DSD_RIGHT_SDATA_OUT	28	O	***I2S serial data output :*** 3.3V TTL output, refer to I2S Specification. ***DSD serial right data (channel 1) output:*** 3.3V TTL output, refer to DSD Specification.
I2S_SCLK_OR_DSD_SCLK_OUT	29	O	***I2S serial clock output:*** 3.3V TTL output, refer to I2S Specification. ***DSD serial clock output:*** 3.3V TTL output, refer to DSD Specification.
I2S_MCLK_DAC	30	O	***I2S master clock output:*** 3.3V TTL output, refer to DAC Document.
DVDD_33_PAD_C	31	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
DVSS_PAD_C	32	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
AVSS_LPLL	33	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
AVDD_12_LPLL	34	P	***1.2V Core Power Connection:*** Power supply for all digital and audio PLL function. Connect to 1.2V.
UART_TX_OR_GPIO_A6	35	I/O	***UART transmitter output:*** 3.3V TTL output, refer to RS232 Specification. ***General purpose input/output pin bank_A[6] :*** 3.3V TTL input/output pin, define by internal control register.
UART_RX_OR_GPIO_A7	36	I/O	***UART receiver input:*** 3.3V TTL input, refer to RS232 Specification. ***General purpose input/output pin bank_A[7] :*** 3.3V TTL

Pin Name	Pin No.	Type	Description
			input/output pin, define by internal control register.
SPI_CLK_AND_POR_0	37	I/O	***SPI interface clock :*** 3.3V TTL output, refer to SPI flash memory Specification. ***Power on latch selection pin 0:*** 3.3V TTL input, reserved for internal software
SPI_DATA_W_AND_POR_1	38	I/O	***SPI interface data output :*** 3.3V TTL output, refer to SPI flash memory Specification. ***Power on latch selection pin 1:*** 3.3V TTL input, reserved for internal software
SPI_WP_Z_AND_POR_2	39	I/O	***SPI interface write protected (low active):*** 3.3V TTL output, refer to SPI flash memory Specification. ***Power on latch selection pin 2:*** 3.3V TTL input, reserved for internal software
SPI_DATA_R	40	I	***SPI interface data input:*** 3.3V TTL input, refer to SPI flash memory Specification.
SPI_CS_Z_AND_POR_3	41	I/O	***SPI interface chip selection (low active):*** 3.3V TTL output, refer to SPI flash memory Specification. ***Power on latch selection pin 3:*** 3.3V TTL input, reserved for internal software
PWM2_OR_GPIO_B2	42	I/O	***PWM2 light control output :*** refer to programming guide ***General purpose input/output pin bank_B[2] :*** 3.3V TTL input/output pin, define by internal control register.
SPDIF_0_OUT	43	O	***SPDIF play channel 0 output:*** 3.3V TTL output, refer to SPDIF Specification.
DVDD_12_CORE	44	P	***1.2V Core Power Connection:*** Power supply for all digital function. Connect to 1.2V.
DVSS_PAD_D	45	G	***Ground Connections:*** Connect all ground pins to the common system ground plane.
DVDD_33_PAD_D	46	P	***3.3V Pad Power Connection:*** Power supply for I/O buffer. Connect to 3.3V.
PWM1_RIGHT_OR_GPIO_B3	47	I/O	***PWM1 light control output :*** refer to programming guide ***General purpose input/output pin bank_B[3] :*** 3.3V TTL input/output pin, define by internal control register.
CLK_REF_OR_GPIO_B4	48	I/O	***XTAL reference clock output :*** refer to programming guide ***General purpose input/output pin bank_B[4] :*** 3.3V TTL input/output pin, define by internal control register.

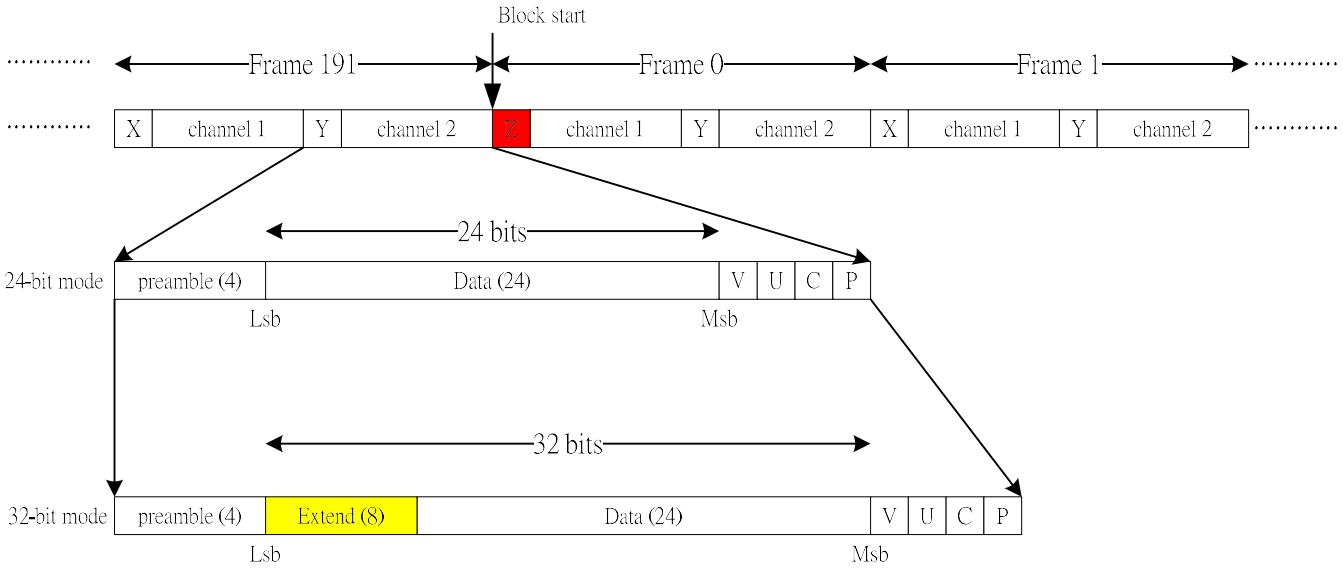
*Note: Internal 120K *pull-up or #pull down resistors present on inputs marked with *# respectively. Design should not rely solely on internal pull-up or pull down resistor to set I/O pins high or low respectively.*

ELECTRICAL CHARACTERISTICS

DC specifications

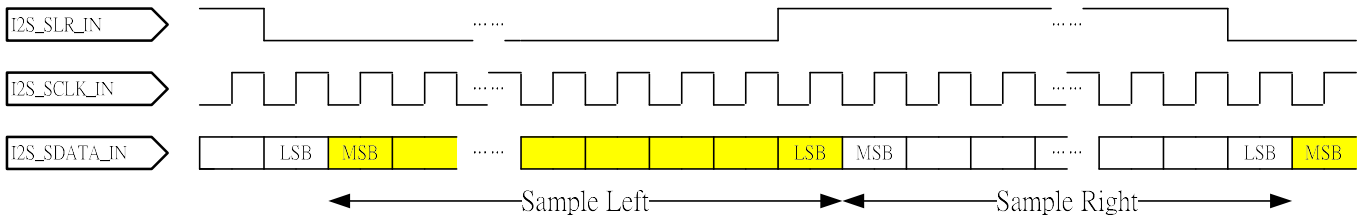
Symbol	Parameter	Min.	Max.	Units	Notes
Absolute VDD CORE	1.2V core supply Voltage	-0.5	1.32	V	
Absolute VDD I/O	3.3V I/O supply Voltage	-0.5	3.6	V	
Ts	Storage Temperature	-65	150	°C	
Ta	Ambient Temperature	0	70	°C	
Absolute Vih	3.3V input high voltage	-0.5	3.6	V	
Absolute Vil	3.3V input low voltage	-0.5		V	
ESD	Input ESD protection	2		KV	Human body mode
Operating Vdd CORE	1.2V core supply Voltage	1.08	1.32	V	
Operating Vdd I/O	3.3V I/O supply Voltage	3.135	3.465	V	
Operating Vih	3.3V input high voltage	2.0	Vdd+0.3	V	
Operating Vil	3.3V input low voltage	Vss-0.3	0.8	V	
Operating Iil	Input leakage current	-5	+5	uA	
Operating Voh	3.3V output high voltage	2.4		V	Ioh=-1mA
Operating Vol	3.3V output low voltage		0.4	V	Iol=1mA
Cin	Input pin capacitance		5	pF	
Cxtal	XTAL pin capacitance	13.5	22.5	pF	17..20 pF
Cout	Output pin capacitance		6	pF	
Lpin	Pin inductance		7	nH	
Operating Current	3.3V active supply current		12	mA	PCM 768K/32bit In/Out
	1.2V active supply current		18	mA	PCM 768K/32bit In/Out
Power down	3.3V supply current		0.29	mA	
	1.2V supply current		0.18	mA	
SPDIF Rx Input Sensitivity		0.100	3.300	V	

SPDIF interface

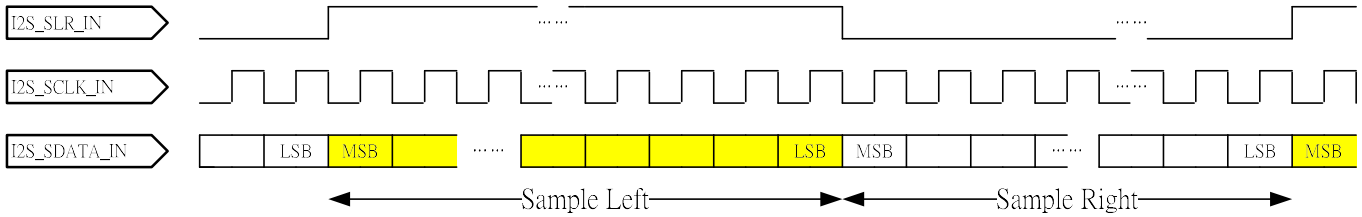


I2S interface

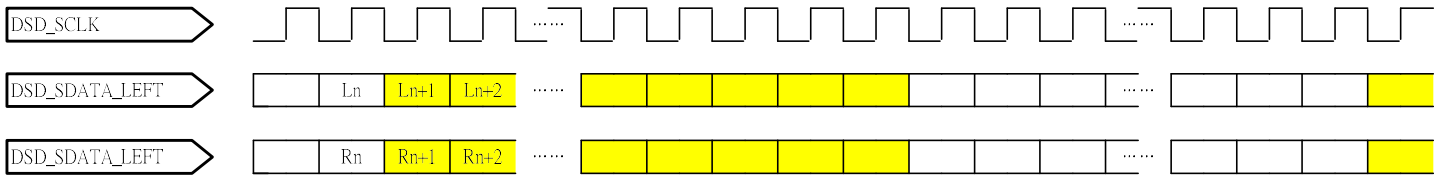
I2S standard format



I2S left justified format

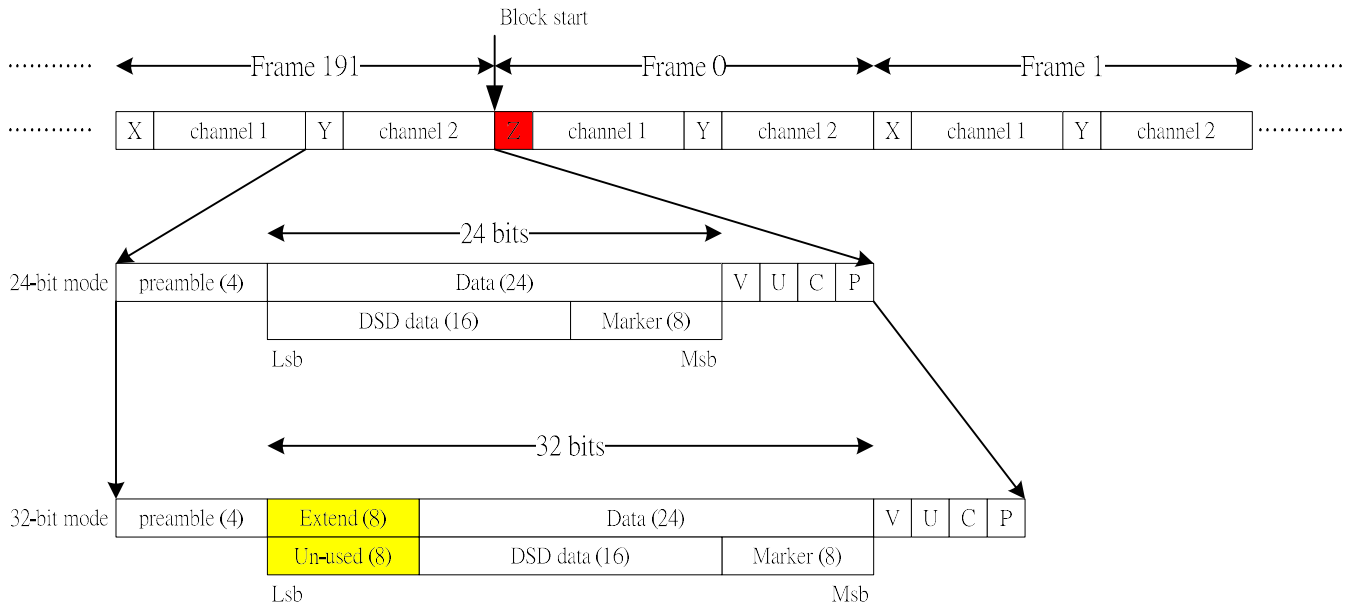


DSD interface



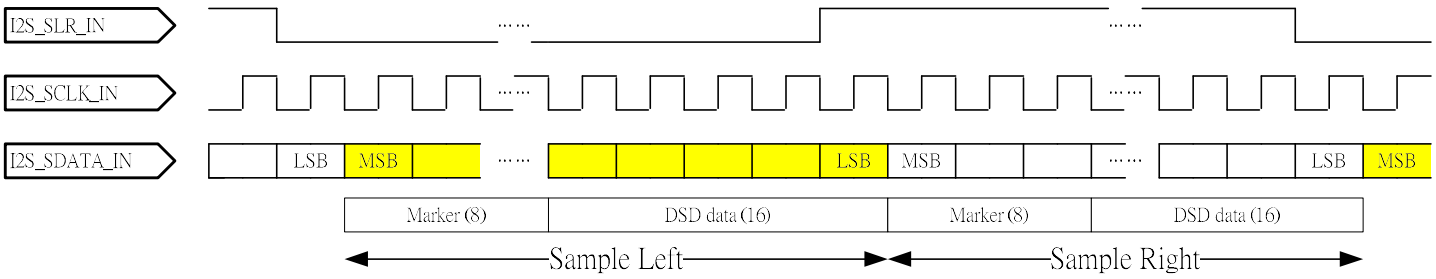
DoP interface

DSD over PCM through SPDIF

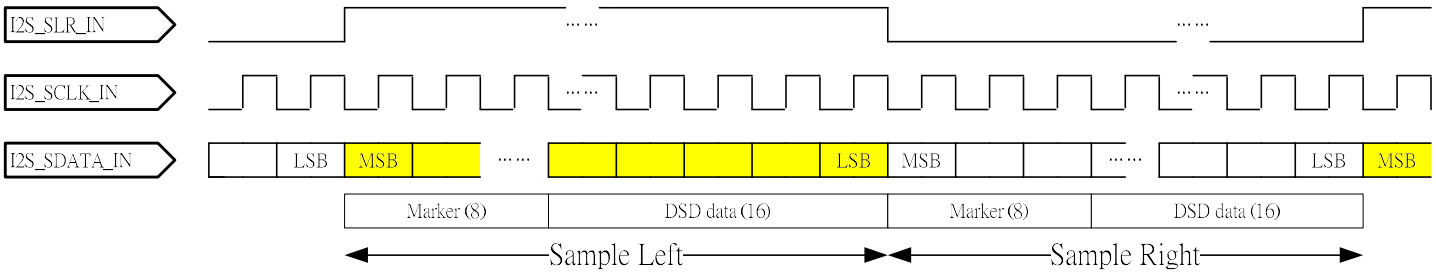


DSD over PCM through I2S

I2S standard format



I2S left justified format



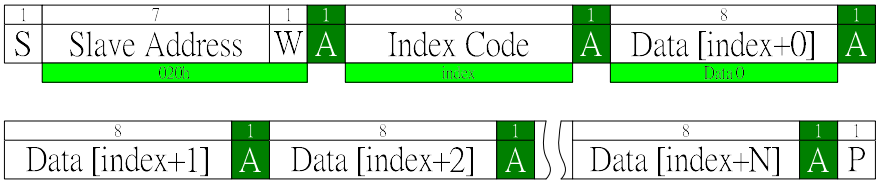
I2C interface

Register write command :

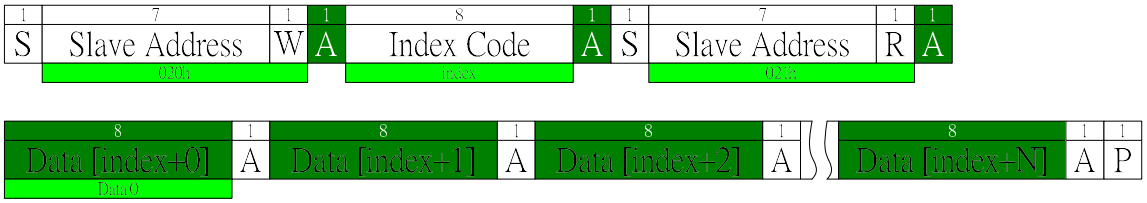
Slave address = 0x28

Register read command :

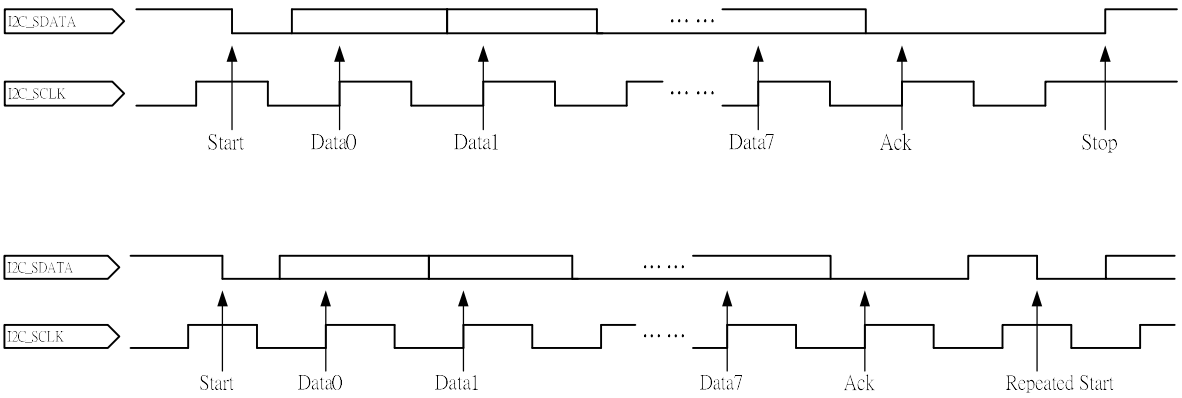
Slave address = 0x29



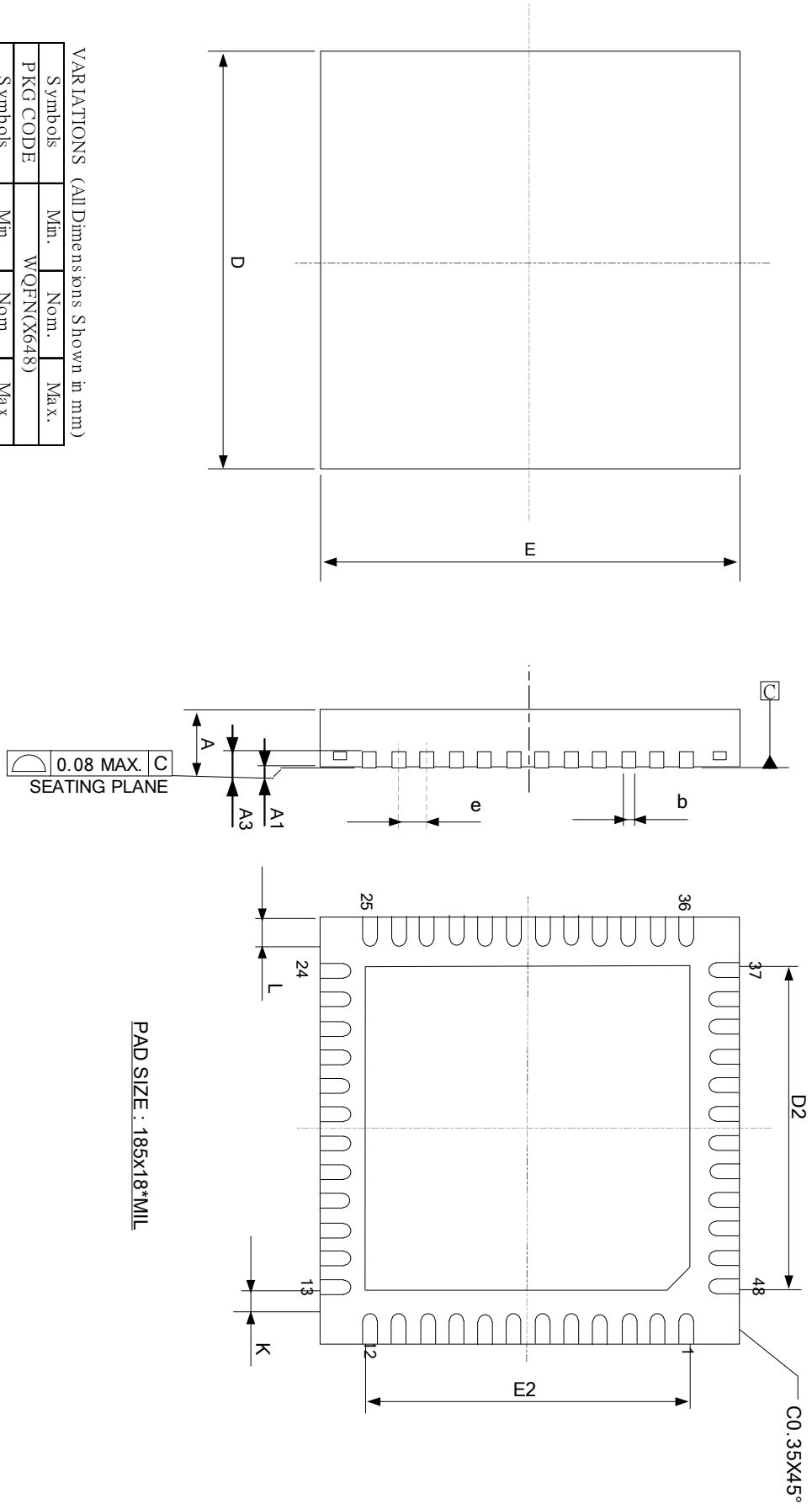
Block Write



Block Read



Package outline QFN 48 pins



VARIATIONS (All Dimensions Shown in mm)

Symbols	Min.	Nom.	Max.
PKG CODE		WQFN(X648)	
Symbols	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		6.00 BSC	
E		6.00 BSC	
e		0.40 BSC	
K	0.20	-	-

PAD SIZE	D2			E2			L		
185X18*MIL	Min.	Nom.	Max.	Min.	Nom.	Max.	Min.	Nom.	Max.
	4.45	4.50	4.55	4.45	4.50	4.55	0.35	0.40	0.45